What is claimed is:

1. A telephone line interface circuit, the circuit comprising:

a differential transconductance amplifier having inverting and non-inverting inputs, a single ended output and first and second differential outputs, where the inverting input is coupled to a first terminal of the telephone line pair through a first series of high resistance value resistors, the non-inverting input is coupled to a second terminal of the telephone line pair through a second series of high resistance value resistors, and the second differential output is coupled to an output terminal of the circuit;

a common mode canceling transconductance amplifier having inverting and non-inverting inputs and first and second differential outputs, where the inverting input of the common mode canceling transconductance amplifier is coupled to the second terminal of the telephone line pair through the second series of high resistance value resistors, the non- inverting input of the common mode canceling transconductance amplifier is configured to receive a first reference voltage, the first differential output and the inverting input of the common mode canceling transconductance amplifier are coupled, and the second differential output of the common mode canceling transconductance amplifier is coupled to the inverting input of the differential transconductance amplifier;

a gyrator transconductance amplifier having inverting and non-inverting inputs and first and second differential outputs, where the inverting input of the gyrator transconductance amplifier is coupled to the single ended output of the differential transconductance amplifier, the non- inverting input of the gyrator transconductance amplifier is configured to receive a second reference voltage, the first differential output of the gyrator transconductance amplifier is coupled to the inverting input of the common mode canceling transconductance amplifier, and the second differential output of the gyrator transconductance amplifier is coupled to the output terminal of the circuit; and

a capacitor coupled between the inverting input of the gyrator transconductance amplifier and a power supply terminal.

2. The circuit of claim 1, the circuit further including a pulse width modulation (PWM) analog-to-digital (A/D) converter for converting a current signal at the output terminal of the circuit to a PWM encoded signal.

3. The circuit of claim 2, where the PWM A/D converter includes a control circuit for generating non-overlapping clock and control signals and PWM conversion circuitry, where the non-overlapping clock and control signals drive the PWM conversion circuitry to generate a comparison output signal responsive to the current signal at the output terminal of the circuit, and the control circuit generates the non-overlapping clock and control signals and the PWM encoded signal responsive to a reference clock signal and the comparison output signal.

4. The circuit of claim 1, the circuit further including a switch disposed between the singled ended output of the differential transconductance amplifier and both the inverting input of the gyrator transconductance amplifier and the capacitor.

5. The circuit of claim 4, where the capacitor is a component of an integrated circuit that includes the differential transconductance amplifier, the common mode canceling transconductance, and the gyrator transconductance amplifier.

6. The circuit of claim 1, where the capacitor is an external component to an integrated circuit that includes the differential transconductance amplifier, the common mode canceling transconductance, and the gyrator transconductance amplifier.

7. The circuit of claim 1, where the high resistance value resistors are 1% tolerance resistors.

8. A method for interfacing to a telephone line, the method comprising the steps of:

developing currents at circuit nodes T and R that are proportional to an input common mode voltage between Tip and Ring terminals of the telephone line;

canceling a common mode signal at circuit nodes T and R by generating a differential pair of common mode current signals from a common mode signal present at circuit node T;

generating a set of current signals that are proportional to a difference signal current at circuit node R that is representative of a differential voltage between Tip and Ring;

generating a direct current (DC) canceling current from a first one of the set of current signals that are proportional to a difference signal current at circuit node R; and

adding the DC canceling current to circuit node T.

9. The method of claim 8, the method further including the step of providing a frequency response pole having a predetermined cut-off frequency.

10. The method of claim 8, the method further including the step of generating a DC current and polarity signal proportional to the voltage between Tip and Ring from

another one of the set of current signals that are proportional to a difference signal current at circuit node R.

11. The method of claim 10, the method including the step of converting the DC current and polarity signal to a pulse-width-modulation (PWM) encoded signal.

12. The method of claim 8, the method including the step of converting one of the set of current signals that are proportional to a difference signal current at circuit node R to a pulse-width-modulation (PWM) encoded signal.

13. The method of claim 8, where the step of generating a set of current signals includes the step of canceling the difference signal current at circuit node R using a second one of the set of current signals;

14. The method of claim 8, where the step of canceling a common mode signal further comprises the steps of:

comparing the common mode signal at circuit node T to a first reference voltage in order to generate a negative feedback current and a common mode current;

adding the negative feedback current to circuit node T; and

adding the common mode current to circuit node R.

15. The method of claim 8, where the step of developing currents at circuit node T and R further comprises electrically coupling to the Tip and Ring terminals through a network of high resistance value resistors.

16. The method of claim 8, where the step of canceling a common mode signal at circuit nodes T and R by generating a differential pair of common mode current signals from a common mode signal present at circuit node T includes generating the differential pair of common mode current signals using a transconductance amplifier.

17. The method of claim 8, where the step of generating a set of current signals that are proportional to a difference signal current at circuit node R that is representative of a differential voltage between Tip and Ring includes generating the set of current signals that are proportional to the difference signal current at circuit node R using another transconductance amplifier.

18. The method of claim 8, where the step of generating a direct current (DC) canceling current from a first one of the set of current signals that are proportional to a difference signal current at circuit node R includes generating the DC canceling current using still another transconductance amplifier.

19. The method of claim 8, the method including the step of converting one of the set of current signals that are proportional to a difference signal current at circuit node R to Caller ID data.

20. The method of claim 8, the method including the step of converting one of the set of current signals that are proportional to a difference signal current at circuit node R to a digital output signal representing DC voltage level and voltage polarity.

21. A telephone line interface device, the device comprising:

high resistance interface means for developing currents at circuit nodes T and R that are proportional to an input common mode voltage between Tip and Ring terminals of the telephone line;

common mode canceling transconductance amplifying means for canceling a common mode signal at circuit nodes T and R by generating a differential pair of common mode current signals from a common mode signal present at circuit node T;

differential transconductance amplifying means for generating a set of current signals that are proportional to a difference signal current at circuit node R that is representative of a differential voltage between Tip and Ring; and

gyrator transconductance amplifying means for generating a direct current (DC) canceling current from a first one of the set of current signals that are proportional to a difference signal current at circuit node R and adding the DC canceling current to circuit node T.

22. The device of claim 21, the device including low noise voltage and current bias source means for biasing the common mode canceling transconductance amplifying means, the differential transconductance amplifying means, and the gyrator transconductance amplifying means.

23. The device of claim 21, the device including pulse-width-modulation (PWM) encoding means for converting the DC current and polarity signal to a pulse- PWM encoded signal.

24. The device of claim 23, where the PWM encoding means further includes:

control means for generating non-overlapping clock and control signals; and

PWM conversion means for generating a comparison output signal responsive to the DC current and polarity signal under control of the non-overlapping clock and control signals,

where the control means generates the non-overlapping clock and control signals and the PWM encoded signal responsive to a reference clock signal and the comparison output signal.